IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)
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MIZUNO	)
	)
Application Number: To be assigned	)
	)
Filed: Concurrently Herewith	)
	)
For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE	)
	)
ATTORNEY DOCKET NO. HITA.0419	)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

The above-referenced application is a continuation of U.S. Serial No. 10/350,084, filed on January 24, 2003. It includes the same disclosure as U.S. patent application Serial No. 10/350,084.

It is understood that the listed references will be considered in the examination of the application and that no separate copies of the same prior art are required to be provided since they were previously cited or transmitted in the foregoing prior application under 37 CFR Section 1.98(d). Form(s) PTO 1449 is enclosed listing references cited by the Examining Attorney and submitted by applicant in the prior applications.

This Information Disclosure Statement is submitted with the above-captioned U.S. continuation application. Accordingly, no fee is due or payable at this time.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 08-1480.

Respectfully submitted,

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Form PTO 1449	ATTY. DOCKET NUMBER	SERIAL NUMBER
	HITA.0419	To be assigned
U.S. Department of Commerce Patent and Trademark Office	APPLICANT Mizuno	
Information Disclosure Statement by Applicant	FILING DATE Concurrently herewith	GROUP

U.S. Patent Documents

Examiner Initial	Cited by Examiner in Parent	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	X	6,107,700	8/22/2000	Ishikawa et al			11/13/98
	X	5,724,297	3/3/98	Noda et al.			12/12/96
	X	5,614,847	3/25/97	Kawahara et al.			8/24/94
	X	5,606,265	2/25/97	Sakata et al			3/21/96
	X	5,583,457	12/10/96	Horiguchi et al.			2/8/94

Foreign Patent Documents

Examiner Initial		DOCUMENT NUMBER	FILING DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
							YES	NO
	AA	8-152945	11/28/94	Japan			Abstract	X

Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

	AB	Shekhar Borkar, *Design Challenges of Technology Scaling,* July-August 1999 IEEE, pp. 23-29
	AC	Jerry M. Soden, Charles F. Hawkins and Anthony C. Miller, *Identifying defects in deep-submicron CMOS Ics, IEEE Spectrum, September 1996,* pp. 66-71
	AD	Takeshi Sakata, Masashi Horiguchi and Kiyoo Itoh, *Subthreshold-current reduction circuits for multi-gigabit dram's*, Central Research Laboratory, Hitachi, Ltd. , pp. 45-46
	AE	Takashi Inukai and Toshiro Hiramoto, *Suppression of Stand-By tunnel Current in Ultra-Thin Gate Oxide MOSFETs by dual Oxide Thickness MTCMOS(DOT-MTCMOS)*, 1999 International Conference of Solid State Devices and Materials, Tokyo, pp.264--265
	AF	Katsuhiro Seta, Hiroyuki Hara, Tadahiro Kuroda, Mazakazu Kakumu, and Takayasu Sakurai, *50% Active-Power Saving without Speed Degradation using Standby Power Reduction (SPR) Circuit*, 1995 IEEE International Solid State Circuits Conference, pp. 318-319
	AG	Maurice J. Bach, *The Design of the Unix Operating System*, Prentice Hall, Inc. , 1986 by Bell Telephone Laboratories, pp. 210-263

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation is considered, whether or not citation is in conformance with MPEP 609; draw a line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant

PTO1449